1. Instructor

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Office hours: Tuesday 12:00 – 13:00, Wednesday 15:00 – 16:00, Thursday 11:00 – 12:30

2. Course Objectives

To learn the fundamental principles needed to analyze and design digital logic circuits, both combinational and sequential. The course focuses on digital design methodologies and the use of computer-aided design tools. Also the students will learn how to interpret and write documentation for digital circuits.

3. Time and Place

• TR: 11:00 – 12:15, Bechtel 537

4. Prerequisites

• EECE 210 – Electric Circuits

5. Textbook


6. Course Topics

• Introduction (Ch. 1): Analog versus digital, Digital devices, Electronics and software aspects of digital design, Programmable logic devices, Digital design levels.

• Number Systems and Codes (Ch. 2): Positional number systems, Octal and hexadecimal numbers, General positional number system conversions, Addition and subtraction of non decimal numbers, Representation of negative numbers,
Two’s complement addition and subtraction, Binary codes for decimal numbers, Gray code.

- Combinational Logic Design Principles (Ch. 4): Switching algebra, Combinational-circuit analysis, Combinational circuit synthesis, Programmed minimization methods, Timing hazards.

- Hardware Description Languages (Ch. 5): HDL-based digital design, The VHDL hardware description language, Basic data types, Structural design elements, Behavioral design elements, Data flow design elements.

- Combinational Logic Design Practices (Ch. 6): Circuit timing, PLDs, Decoder, Encoders, Multiplexers, Exclusive OR and parity circuits, Comparators, Adders, Subtractors, ALUs.

- Sequential Logic Design Principles (Ch. 7): Latches and flip-flops, Clocked synchronous state machines, Designing state machines using state diagrams, VHDL sequential-circuit design features.

- Sequential Logic Design Practices (Ch. 8): Counters, Shift-registers.

- Memory (Ch. 9): Read-Only Memory, Read/Write Memory SRAM, DRAM.

7. **Student Assessment and Grading**

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7.1. **Participation:** This includes class attendance. You are expected to attend all classes. You are responsible for the work done and for the announcements made during your absence. The participation grade will be based on the statistics collected from taking class attendance. You get 5 for less than two absences, 4 for two absences, 3 for 3 absences, 2 for 4 absences, 1 for 5 absences, and 0 for more than 5 absences. In case you have a valid excuse for not attending a class session, you have to send the instructor an email within three days to explain your case.

7.2. **Examinations:**

- The midterm exam will be held on **Monday November 26, 2007 at 18:30**.

- The final exam will be held during the final examination period (between January 22, 2008 and February 2, 2008).

- Exams are subjective and comprehensive.
7.3. **Homeworks:** There will be around *six homeworks* that will cover the main topics of the course. They will consist of problem solving in addition to VHDL programming.

- You are expected to submit your *own solutions* to all assigned homeworks.
- You are required to *hand-write your own solution independently*. Copying is not acceptable and it will result in zero grade to all involved parties.
- You are required to hand in your solutions at the beginning of the class in which they are due. Late submissions are not accepted and will not be graded.
- You have *one week* after grades are announced to request any review of the correction of your homework.
- There will be short quizzes based on homework problems.

7.4. **Projects:** There will be *two project assignments* given throughout the semester. The projects will include digital design problems and will require VHDL programming. You will be required to work in groups of either two or three students.