Minimizing Energy Consumption of SRAM Arrays by Optimally Determining the Data Retention Voltage

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Abstract—This paper presents a new method to minimize the energy consumed by SRAM arrays by optimally measuring the data retention voltage (DRV) that would keep its data integrity during standby mode and in the presence of process variations. The proposed technique relies on implementing an on-chip test circuit to test the integrity of the SRAM array at different voltages. The on-chip test circuit consists of a built-in-self-test (BIST) unit, a DC-DC converter and a Test Control Unit (TCU). The proposed test circuit was implemented in 90nm TSMC technology and simulated using Spectre. Different DRVs were determined for each array depending on the variations present in it. Our circuit showed that the SRAM array under test could be operated at 80mV resulting in considerable energy saving.

I. INTRODUCTION

According to the International Technology Roadmap for Semiconductors 2009 report, power consumption and variability are expected to increase significantly as transistor sizes shrink to 32nm and below [16]. This poses a serious threat on the reliability of the implemented circuits especially circuits that are ratioed such as static random access memory (SRAM) and latches, since such circuits depend sizing their transistors differently to ensure correct operation [17]. At the same time, the demand for integrating more functionalities on-chip has also been increasing especially in mobile applications such as smart phones, iPods, laptops… However, in these applications, battery lifetime imposes a strict limitation on the allowed power consumption of the integrated chip, driving designers to search for new techniques to mitigate the power consumed by the circuits without affecting the performance. Techniques such as dynamic voltage scaling for circuits characterized by varying performance requirements were introduced to address the power problem [8]. Nevertheless, variations in device characteristics limit the power-saving capability of these techniques since they jeopardize system reliability. Furthermore, the random nature of these variations has necessitated the developments of models to predict their effect on circuit performance.

One of the major components of all modern integrated circuits and the main contributors to their power consumption is SRAM memory. To minimize their power consumption, their voltage is stepped down during standby mode to the minimum voltage that would retain their data – the data retention voltage (DRV). However, the DRV is affected by the variations in the SRAM transistors, thus a study of the effect of variations on the DRV was studied in the literature and different approaches – analytical, statistical and both – were introduced in the literature.

Analytical techniques to determine the DRV relied on transistor models and basic circuits’ to derive mathematical models that related the DRV to the threshold voltages of the SRAM transistors at either normal or subthreshold supply voltages [1,2,10,11]. However, such techniques suffer from two major drawbacks. Due to the complexity of the problem, many simplifying assumptions and approximations are performed to keep the problem tractable [1,11]. In many of the proposed techniques, complex models of the cell with no analytical solutions were encountered and numerical approaches were used to derive expressions for the stability measures [2,11]. Such approximations render the results achieved inaccurate and necessitate overestimation of the studied stability measure to account for the inaccuracies. On top of that, these models show the effect of $V_T$ variations on a single cell and cannot be generalized to an SRAM array.

To overcome the limitations of analytical models, statistical techniques were introduced. These techniques rely on simulating the SRAM array for different $V_T$ values and measuring the probability distribution of the DRV. Assuming a certain probability distribution for the threshold voltage, Monte-Carlo (MC) simulations are used to sample values for the threshold voltages of the SRAM transistors. Then, SRAM cells are simulated with these values and the stability measures extracted. Finally, the extracted measures are compared to the failure limits in order to calculate the probability of failure of the SRAM under threshold voltage variations [6].

Even though MC simulation allows the simultaneous variation of all threshold voltages in an SRAM, it samples from the most probable input values, while most SRAM cells fail when the variations are high. Thus, the samples of most
interest are the samples lying in the tail of the threshold voltage distribution. Hence, to accurately estimate the failure probability, billions of samples are required making the technique too slow [6]. Modifications to the standard MC sampling technique, such as Importance Sampling, Mixture Importance Sampling and Statistical Blockade were introduced to allow more sampling in the tail regions and reduce the simulation time [4,5,6,7].

Although these techniques provide good estimates of the stability measures, they necessitate over-estimating the DRV before implementation to account for unstudied cases and approximations. In this paper, an accurate approach to measure the DRV of large SRAM arrays is presented. In this approach, the DRV is measured by implementing a DRV computing circuit that consists of a BIST unit, DC-DC converter and control circuitry. The rest of the paper is organized as follows. Section II presents an overview of the general framework implemented to determine the DRV, then section III describes the BIST unit, section IV describes the Test Control Unit (TCU), and section V presents the results achieved and concludes the paper.

II. THE GENERAL FRAMEWORK

In the proposed technique, the minimum energy point of an SRAM array is assumed to be at the data retention voltage. Thus, the main aim of the implemented on-chip test circuit – the DRV computing circuit – is to determine that voltage accurately when the chip is in test mode. Once the DRV is determined, the DRV computing circuit saves it and supplies it to the array when the array is in standby mode. To do that, the DRV computing circuit must contain a DC-DC converter, a BIST unit capable of determining data retention faults and a test control unit (TCU). The DRV computing circuit checks the integrity of the SRAM data at different voltages. If the array passes the check at a particular voltage, the voltage is lowered and the test is repeated. When the array fails, the DRV is determined as the voltage step above the current voltage. Fig. 1 shows the general setup of the DRV computing circuit during test mode.

The TCU controls the DRV computing procedure and saves it: It supplies the low power DC-DC converter with the reference voltage that should be supplied to the SRAM array. The TCU chooses $V_{ref}$ according to the SRAM operating mode: $V_{ref}$ is set to the nominal voltage $V_{Bat}$ during read and write operations or to the determined DRV during standby mode. However, when the chip is in test mode, the TCU sets $V_{ref}$ to voltage step currently being tested. The DC-DC converter regulates its output voltage to $V_{ref}$ with the help of the comparator and analog-to-digital converter. The converter must be able to efficiently provide a wide voltage range, thus the switched capacitor DC-DC converter proposed in [13] is used. The SRAM BIST unit implements a testing algorithm that determines if the array fails at a specific retention voltage. The BIST unit will be discussed in more details in section III; whereas the TCU in more details in section IV.

III. THE PROPOSED BIST UNIT

The main job of the BIST unit implemented within the DRV computing circuit is to test for and detect data retention faults, in addition to detecting the usual memory faults. Data retention tests require saving known data within the memory and retaining it for a period of time before testing the memory again to check its retention capabilities. The most effective and commonly implemented memory test algorithm is the March C-test. However, this test algorithm is incapable of detecting data retention faults. A modified version of the March C-algorithm, known as IFA-9, introduces delays after the last two write operations to detect retention faults. Fig. 2 shows the IFA-9 algorithm. The recommended delay time is 100 ms [14]. To count this delay, a Delay Counter block is implemented within the DRV computing circuit. The Delay Counter block need not be developed on-chip; the processor available on-chip could be used to count the required delay.

Figure 1: DRV computing circuit in test mode
The SRAM BIST unit within the DRV computing circuit implements a more condensed form of the IFA-9 algorithm. Since the BIST unit should test the array at each voltage step, the full algorithm can be run once at the original supply voltage to detect the different fault classes, while the algorithm shown in Fig. 3 is repeated for every voltage step to ensure the retention of data at that step. Thus, the algorithm will write zero to all memory locations before lowering the SRAM supply voltage to the voltage step-under-test. The supply voltage is retained for a delay of 100ms before it is increased or decremented.

In the proposed circuit, the BIST unit is designed as a state machine representing the different steps of the DRV test algorithm. Other BIST unit designs can be used, however, this particular design was chosen because it takes up little area on-chip. Fig. 4 shows the different blocks in the BIST unit and how they interact. The Pattern Generator is responsible for controlling the test procedure; it provides the SRAM array with the Read/Write signals and the data to be written (DataToWrite), the Address Generator with the order in which the array should be accessed (Inc/Dec Address), and the Comparator with the data that should be read (DataToRead) from the array. The Pattern Generator collects the results of the read operations from the Comparator through the signal PassFail. To account for the delay element in the test procedure, the Pattern Generator provides the remote Delay Counter with the enable signal, DelayCntEn, and reads from it the end of the delay interval through the signal Continue. The signal ReinitState resets the Pattern Generator to its initial state; whereas, the signal TestPass indicates the array has passed the tests that were carried out on it and TestDone signals the end of the test procedure. The Address Generator is responsible for providing the array with the address of the cell that is currently being accessed. It takes from the Pattern Generator two signals: the Reset signal responsible for resetting the address to initial value and the Inc/Dec Address signal that indicates whether the address should be incremented or decremented.
QuitTest signal is set and the TCU will save that voltage within a register and use it whenever the array enters standby mode.

Within the TCU, the register DRV holds during test mode the value of the voltage-step under test and is updated whenever the SRAM array passes the DRV test. When the SRAM array passes the DRV test for a particular voltage, the TCU lowers the voltage by one step (DRV := VStep) and saves it within the register. If the SRAM array fails, the TCU raises the voltage by one step (DRV += VStep), saves it and repeats the procedure again. If the test passes, the DRV computing circuit has completed its task and the TCU sets the flag QuitTest to signal that. Otherwise, the voltage is stepped up and the procedure is repeated again until the array passes the DRV test.

V. IMPLEMENTATION AND RESULTS

The hardware was first verified using Cadence Spectre. The SRAM array, BIST and TCU units of the DRV computing circuit were implemented in Cadence Virtusuo using TSMC 90nm technology. The DC-DC converter and ADC were implemented using Verilog-A. Monte-Carlo simulation for 100k VT samples was performed and the DRV was determined as 150mV. This result was then used to study the effectiveness of the proposed DRV computing circuit.

![TCU flowchart](image)

Figure 5: TCU flowchart

The proposed circuit was simulated multiple times with different sets of V_Ts for the cell transistors and the DRV was computed. SRAM arrays with different sets of VTs resulted in different DRVs ranging from 100mV to 200mV summarized in Fig. 6. While the previously used techniques fixed the DRV at 150mV, the proposed circuit assures the integrity of some SRAM array at 100mV thus saving considerable power. Furthermore, the proposed circuit consumes little extra area, since BIST units and DC-DC converters are already becoming a major component of all chips; so, the only area overhead comes from the implementation of the TCU and the additional delay test in the BIST algorithm.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Result</th>
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<tr>
<td>Set 1</td>
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<tr>
<td>Set 2</td>
<td>100mV</td>
</tr>
<tr>
<td>Set 3</td>
<td>150mV</td>
</tr>
<tr>
<td>Set 4</td>
<td>150mV</td>
</tr>
<tr>
<td>Set 5</td>
<td>200mV</td>
</tr>
</tbody>
</table>

Figure 6: Results

REFERENCES


