Energy-Efficient Cascaded Bit-Interleaving Protocol for Integrated Optical Access/In-Building Networks

Tolga Ayhan, Ahmad R. Dhaign, Leonid G. Kazovsky
Photonics and Networking Research Laboratory
Stanford University
Stanford, CA, USA

Dusan Suvakovic, Hungkei K. Chow
Alcatel-Lucent Bell Labs
NJ, USA

Abstract— This paper proposes and experimentally evaluates the Cascaded Bit-interleaving architecture and protocol, an energy-efficient solution that aims to reduce the power consumption of integrated optical access/in-building networks, while offering high-speed Internet service to end-users. In the new architecture, optical-electrical-optical (OEO) regeneration is employed at the interface between the access and in-building networks, and downstream frames are generated at the central office using the two-stage bit-interleaving scheme. The users’ network nodes only process the data destined for them without any buffering at a lower clock rate than the aggregate PON rate, thereby significantly reducing their energy consumption. Simulation and experimental results demonstrate the proof of concept and show that the power consumption of the access/in-building network can be significantly reduced when the proposed cascaded bit-interleaving protocol is employed.

Keywords—Optical Networks, Energy Efficiency, PONs, Protocols

I. INTRODUCTION

Energy efficiency in communication networks has become a very important subject due to the explosive growth in the number of users and the demand for higher data rates per user. It is predicted in [1] that by year 2018, communication networks will consume about an order of magnitude more power than today unless disruptive improvements in the energy efficiency are achieved. Therefore, it is essential to reduce the power consumption of communication networks while at the same time providing high data rates to end-users. Specifically, decreasing the power consumption of access networks in general and of optical access and in-building networks in particular has become an urgent need, as these networks constitute the largest part of the Internet and connect a very big amount of active devices.

Passive optical network (PON) has been considered an attractive technology for broadband access networks [2]. It comprises an Optical Line Terminal (OLT) that resides in a Central Office (CO) and connects a set of associated Optical Network Terminals (ONTs) through a single fiber after being fed via a remote node (RN) in which a passive power splitter is employed. Time division multiple access (TDMA)-based PONs, such as Ethernet PON (EPON) and Gigabit PON (GPON), have been standardized, and they employ one wavelength in the upstream (i.e., from ONTs to OLT) and another wavelength in the downstream (i.e., from OLT to ONTs). Existing PON protocols are not optimized in terms of energy-efficiency. Therefore, it is important to design the protocol with the goal of achieving energy-efficiency while at the same time satisfying the data rate and quality-of-service (QoS) requirements. Various solutions have been proposed in the literature aiming at reducing the power consumption of PONs. One promising technique is to enable the sleep mode operation at the ONT, and perform dynamic power management [3, 4]. However, the amount of reduced power has not been as great as desired.

In TDM-PON, downstream frames are formed at the OLT and are broadcast to all ONTs. Thus the ONT processes all downstream frames at the line rate of the PON, and subsequently if the destination address does not match the ONT’s address, it drops the frame. This mechanism significantly impacts the power consumption of PON [4], since it forces the ONT to perform unnecessary frame processing for the biggest part of the incoming traffic.

Consequently, bit-interleaving was proposed as an effective solution for mitigating this problem [5]. In bit-interleaving passive optical network (Bi-PON), the downstream frame’s payload is interleaved at the OLT and broadcast in the downstream direction, and each ONT processes its designated payload bits at a low rate, and thus it drops all other payload bits without processing them. This reduces the average power consumption for protocol processing in the ONT by more than an order of magnitude. Taking into account the consumption of other components like the optical transceiver and home gateway processing, the total power consumption of the ONT can be reduced by about 67% in a 10 Gbps PON [6].

Today, Internet service providers such as Verizon FiOS terminate the PON at the ONT and employ a Multimedia-Over-Coax (MOCA) in the building [7]. A straightforward approach to make the network more energy-efficient could be to replace the MOCA in home with an in-building PON. However, this approach would not be good since the ONT in this case has to behave as both an ONT terminating the WAN PON and an OLT serving the LAN PON. That would raise complexity and cost issues and increase the power consumption of the ONT. Therefore in this paper, we propose a protocol that allows for a very simple ONT architecture (which we refer to as Repeater), which helps reduce the power
consumption. It is also known that the power consumption of in-building networks is a significant contributor to the overall power consumption of communications networks, especially with the increase in demand for very high-speed services. Therefore, we envision an integrated access/in-building network with centralized processing at the central office, which reduces the processing overhead of the customer premise equipment (CPE) and decrease the total energy consumption in the network.

In this paper, we propose a cascaded bit-interleaving architecture and protocol for the integrated optical access/in-building network. The proposed architecture replaces the ONT with the Repeater and extends the optical distribution network to penetrate the in-building network, which terminates at an end-ONT residing inside the building. The new architecture implements the bit-interleaving technique to reduce the energy consumption of the ONT. It also centralizes the routing function at the OLT to further decrease the end-ONT power consumption. Furthermore, the clock rate is decreased at the interface in the CPE to make the overall network even more energy efficient.

The rest of this paper is organized as follows. In Section II, we describe the proposed Cascaded Bit-Interleaving architecture and protocol. This includes a detailed description on the structure of the repeater and end-ONT, as well as how the downstream frame is generated at the OLT. In Section III, we discuss the energy savings achieved using our proposed architecture. In Section IV, we present our simulation and experimental results, which highlight the merits of the proposed solution. Section V concludes the paper.

II. CASCADED BIT-INTERLEAVING PROTOCOL

In this section, the proposed integrated access/in-building network is presented. The network nodes and their building blocks are also detailed. The proposed downstream transmission protocol is explained, and the frame generation strategy at the OLT is described. The upstream control protocol is the same as the legacy PON upstream protocol, and is supported in the proposed scheme via embedding the upstream control information in the downstream frame header.

A. Network Architecture

The proposed integrated access/in-building network architecture is illustrated in Fig. 1. We employ passive optical networks in both access and in-building networks, such that there is optical-electrical-optical (OEO) regeneration at the repeater. We consider the downstream data rate to be 10 Gbps for the access network and 1 Gbps (peak) for the in-building network. We design the cascaded bit-interleaving protocol for the combined access/in-building network. The repeater provides the interface between the access and in-building networks. The end-ONT can be considered as a network interface unit connected to the end-user’s terminal.

B. General Downstream Frame Structure

The downstream frame in the proposed architecture is generated at the OLT and broadcast to all repeaters. The frame consists of a header section and a payload section. The header section consists of a constant synchronization bit pattern, ONT IDs, and downstream and upstream bandwidth map. The downstream bandwidth map contains the flag, decimation rate and offset information so that when a network unit starts getting its payload bits, it can locate its designated bits from the already interleaved payload block. The general architecture of a downstream frame is illustrated in Fig.2. A specific lane, which is associated with an ONT-ID, is described by the horizontal bar in the header in Fig. 2, and the corresponding payload bits are represented by the small rectangles in the payload section. It should be noted that the payload bits of a node are defined by the rate and offset information extracted from the downstream bandwidth map associated with the node’s ONT-ID number. The frame structure shown in Fig.2 is based on a fixed number of ONT-IDs.

C. Repeater and End-ONT Structures

The building blocks of the repeater are provided in Fig.3. The receiving procedure at the repeater can be described as follows: First, the repeater recovers the line rate clock from the access network. Next, it decimates received bit stream at the rate of 1/N, where N is the number of repeaters in the network. The repeater searches for a synchronization pattern from the decimated stream. If it synchronizes successfully, it locks to its own lane (i.e. finds the lane with the associated ONT-ID). Next, the bandwidth map field is descrambled and parsed. Then, the downstream payload flag associated with its ONT ID is extracted from the bandwidth map (BW map) parser, which indicates whether there is any downstream
payload for this repeater from the header. If there is payload data, it fetches the corresponding bits from the payload section of the frame using the rate and offset information that were extracted from the header using the BW map parser. This is done by sending the rate and offset parameters to the decimator. The repeater then forwards the decimated bits to the descrambler. However, if there is no payload data for the corresponding repeater in the current frame, it does not fetch any payload bits and waits for the next frame. The descrambled bits are sent to the Forward Error Correction (FEC) decoder, and then broadcast to the in-building network.

Fig. 3: Building blocks of the repeater

A detailed illustration of the decimator block in the repeater is provided in Fig. 4. To fetch 4 bits from the 32-bit register, the 32:4 multiplexer (MUX) is used at each clock cycle, and similarly to fetch 2 bits from register, the 32:2 MUX is used at each clock cycle. If the decimation rate is between 1/32 and 1/1024, the 32:1 MUX is used at every appropriate number of clock cycles to achieve these decimation rates.

Fig. 4: Decimator block in the repeater

The building blocks of the end-ONT are provided in Fig. 5. Same as the repeater, the end-ONT processes only the necessary parts of the frame’s payload block if it has any downstream data to receive. In addition to the decimator block, a descrambler, and a payload decryption block that are rate adaptive are employed in both the repeater and end-ONT. It should be noted that the bits are descrambled after the decimation, so we need to consider the decimation rate and take it as a parameter to correctly perform the necessary operations for the descrambler and other subsequent blocks. FEC is not applied to the in-building frames due to the short distance between the repeater and end-ONTs. The optical power of the 1Gbps SFP at the repeater (for downstream transmission) can be slightly increased to compensate for that.

Fig. 5: Building blocks of the end-ONT

Fig. 6 gives the internal structure of the decimator block in the end-ONT. For each distinct possible data rate, there is a separate register. The possible decimation rates range from full rate (i.e., rate = 1) to 1/8. When the register (that is at the bottom in Fig. 6) is full, the content is sent to the descrambler block.

D. Frame Generation at the OLT

In the proposed protocol, the OLT performs the following three steps to generate the proper downstream frame for each end-ONT. First, it forms and interleaves the payload blocks for each in-building network, using the decimation rate and offset information of the end-ONTs. These frames consist of a synchronization block, end-ONT id block, downstream bandwidth map that contains the decimation rate and offset, upstream bandwidth map, and the interleaved payload as shown in Fig. 7a. After forming all small frames in step 1, the payload and bandwidth map sections are scrambled and FEC encoder is applied to the scrambled sections as illustrated in Figure 7b in step 2. Then, after all small frames are ready; the OLT interleaves all small frame bits and places them into the payload section of a large frame (i.e., the frame that is sent in the downstream direction of the access network), before scrambling all the parts except for the synchronization and ONT-ID blocks as shown in Fig. 7c. Subsequently, the FEC encoding is performed on the scrambled parts of the frame as the final step.

The OLT assigns time slots for all end-ONTs and repeaters in the network for upstream transmission and inserts this information in the upstream bandwidth map in the header section.
III. ENERGY SAVINGS IN THE PROPOSED ARCHITECTURE

When the cascaded bit-interleaving protocol is used in the integrated access/in-building network, each end-ONT receives only its own payload data, and is able to process at a low clock rate due to the decimation steps at the repeater and end-ONT. Hence, the amount of digital signal processing at the end-ONT is reduced, which contributes to power savings. In addition, the PON interfaces (i.e. SFP, oscillators, PLLs, transimpedance amplifier and limiting amplifier) consume less power in each end-ONT since the data rate is reduced and the distance to the repeater is short (typically less than 100 meters). When there is no data rate reduction at the repeater, the PON interfaces at the end-ONT consumes more power than the case when the decimation is performed at the repeater, due to the fact that when the repeater performs decimation, the line rate at the in-building PON is lower than the access network, hence the end ONTs can have low-clock rate PON interface modules. This makes the proposed network architecture more energy-efficient than one-stage Bi-PON, in which the PON interface has to operate at 10 Gbps.

It should be noted that the repeater is shared among all the end-ONTs in the in-building network, and the complexity of the repeater is reduced since the routing functionality is centralized in the OLT. Centralizing the repeater functionalities at the OLT reduces the repeater power consumption and increases the OLT power consumption; however when the routing functionality is centralized and shared, the total static power consumption and cooling power consumption can be significantly reduced per-user. Also, one OLT replaces the routing functionality in multiple repeaters, thus the power overhead of all repeaters, including interleaving and power supply losses, leakage etc. is eliminated.
IV. PERFORMANCE EVALUATION

In order to test the protocol, the functions of repeater and end-ONT are implemented in VHDL to program FPGAs. The VHDL code is simulated using Modelsim. For different decimation rates, the frame is constructed and taken as an input to the repeater. The output of the repeater is given to the end ONT as input and the output of end ONT is observed for different decimation rates. The transmission is verified using different in-home data rates in the simulation environment.

We use PowerPlay Power Analyzer Tool in Quartus II software using the project files for the repeater and end-ONT separately. The repeater and end-ONT functions are implemented using Altera Stratix IV Field Programmable Gate Array (FPGA). The power consumption values of the FPGA boards are obtained using gate-level simulations in Quartus II. The dynamic power consumption (including the I/O power consumption) estimations of repeater and end-ONT under the proposed Cascaded Bit-interleaving protocol in the integrated access/in-building network are provided in Table I and Table II, respectively. The I/O power consumption is the power consumed by external load capacitors connected to the output pins plus power consumption of the output driver circuits. In the results shown in Table I and Table II, the FEC decoding at the end-ONT are not included. Also, the transceiver interface modules (i.e. the modules that provide the interface between the FPGA fabric and the SFP) are not included in the gate-level simulation results. It should be noted that the access network data rate is 10 Gbps.

<table>
<thead>
<tr>
<th>Decimation Rate (Access Network Data Rate = 10 Gbps)</th>
<th>Dynamic Power Consumption (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/8</td>
<td>118.48</td>
</tr>
<tr>
<td>1/128</td>
<td>81.63</td>
</tr>
<tr>
<td>1/1024</td>
<td>78.45</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Decimation Rate (In-Building Data Rate = 1 Gbps)</th>
<th>Dynamic Power Consumption (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>90.09</td>
</tr>
<tr>
<td>1/2</td>
<td>74.84</td>
</tr>
</tbody>
</table>

Despite the fact that FPGAs are not designed for achieving energy efficiency but rather for providing flexibility and ease of implementing a digital design, the results suggest that we can reduce the power consumption significantly when we use the proposed Cascaded Bit-interleaving protocol as compared to the legacy access/in-building networks. In [5], it is shown that when legacy XGPON protocol is implemented in the access network, the dynamic power consumption of the ONT (which is used instead of a repeater) is 3.6 Watts alone when the in-building rate is 1 Gbps. It can also be observed that the dynamic power consumption of repeater and end-ONT scales well with the decimation rate. In addition to the power savings at the ONT (repeater in the proposed architecture), the proposed Cascaded Bit-interleaving protocol can make the in-building end user equipment energy efficient with the use of proposed end-ONT, thereby providing a low power network interface function to the user’s equipment. It should be noted that the repeater is shared between 8 end-ONTs, so the repeater power penalty per user is (118.48 mW)/8 when the decimation rate at the repeater is 1/8 and the access network data rate is 10 Gbps.

V. CONCLUSIONS

In this paper, we have described the architecture and operation of an integrated access/in-building network based on the Cascaded Bit-interleaving protocol, which aims to reduce the power consumption of integrated optical access/in-building networks. Additionally, we have experimentally demonstrated the energy-efficiency of the proposed scheme. In the proposed architecture, the repeater performs the OEO regeneration and provides the interconnection between the access and in-building networks. The end-ONTs provide network interface to the end user equipment, which can also be a wireless access point. The main advantages of our proposed protocol can be summarized as follows: First, the repeater/end-ONT processes only the data that is destined for it, and not all the data in a passive optical network environment, which is one of the factors making the protocol energy efficient. Furthermore, the repeater/end-ONT processes the payload data at a lower rate than the aggregate rate of the PON (the exact rate depends on the decimation rate), which is another step for achieving high energy-efficiency. Finally, since there is no buffering in repeater or end ONT, the repeater/end ONT consumes less power. We envision the proposed network architecture and protocol to be a promising candidate for future green access/in-building networks.

ACKNOWLEDGMENT

The authors from Stanford University acknowledge Alcatel-Lucent Bell Labs, NJ, USA and NSERC for their support.

REFERENCES

